**Simulation using Synopsys VCS**

1. Place all of the files of the hardware under test, including the Top Module, the Sub Modules, and the Test Bench to a single directory.
2. Make sure that the following commands are available in your test bench code:

**Command 1**: $dumpfile("Module\_Name.vcd");

**Command 2**: $dumpvars(0,Test\_Bench\_Name);

**Notice**: "0" is specified in order to dump the content of all of the existing variables inside the code.

1. Enter the following commands:

**Command 1 (Verilog)**: vcs Module(s)\_No\_Timescale.v Testbench\_With\_Timescale.v -timescale=Specified\_Timescale

**Command 1 (Verilog for File)**: vcs Module(s)\_No\_Timescale.v Testbench\_With\_Timescale.v -timescale=Specified\_Timescale -sverilog

**Command 1 (Netlist)**: vcs Library.v Netlist.v Testbench\_With\_Timescale.v -timescale=Specified\_Timescale

**Command 2**: ./simv

**Command 3**: dve

1. Once Synopsys Discovery Visual Environment (DVE) opened, go to “**File/Open Database**” and then select the “\*.vcd” file.
2. Choose the desired inputs and outputs from the “DUT” part.
3. Right click on them and choose “**Add To Waves/Add To New Wave View**”.